**REMARKS**

The Applicants request reconsideration of the rejection dated February 10, 2006, as follows.

Claims 1-2 and 4-18 are pending.

Claims 1-2 and 4-18 were rejected under 35 U.S.C. 102(e) as being anticipated by Doing, U.S. 2003/0009648 (Doing). The Applicants traverse as follows.

The control unit claimed in Claim 1 includes a first processor which translates a file access into a block access, a second processor which controls the plurality of disk drives on the basis of the block access, a cache memory and a disk interface which connects the second processor and the plurality of disk drives. The control unit logically partitions the host interface, the first processor, the second processor, the cache memory, the disk interface, and the plurality of disk drives, and causes these partitioned elements to operate as a plurality of virtual storages independently.

Doing, on the other hand, does not disclose or fairly suggest the claimed logical partitioning within the storage system. Of particular note is Doing's failure to show the claimed partitioning of the disk interface.

Of further note is the claimed feature that the control unit translates a file access received at the host interface into block access, and controls the plurality of disk drives on the basis of the block access. The Office Action refers to Doing at Paragraph [0055], which discloses a CPU 101 including a storage control portion 221 that accesses data in the L1 data cache or interfaces with memory external to the CPU where instructions or data must be fetched or stored, but does not disclose translation of a received file access into block access. In this regard, the Applicants note the further reference to Paragraphs [0037] and [0047] which allegedly teach the translation, but Doing's real address translation and partitioning is not seen to translate a file access into a block access.

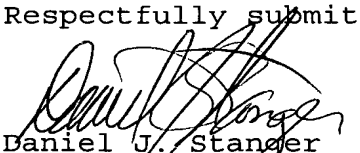
Further, Doing's CPUs 101A, 101B (Fig. 1) constitute separate processors of the multiprocessor computer system 100 for utilizing the disclosed logical partitioning architecture. Doing does not appear to partition CPUs 101A and 101B in the manner required by the claims if CPUs 101A and 101B were to correspond to the claimed first and second processors. More specifically, Doing is not seen to disclose that CPUs 101A, 101B are operated with a host interface, cache memory, disk

interface, and plurality of disk drives, partitioned accordingly, as a plurality of virtual storages independently.

In view of the foregoing amendments and remarks, the Applicants believe that the rejection over Doing has been overcome.

However, the Applicants request an interview with the Examiner to be conducted near the beginning of the month of June 2006 when a representative of the assignee will be in the United States and available for the interview. The Applicants had previously requested this interview during a prior visit, but the Examiner was unavailable at that time. The Applicants' representative will contact the Examiner to schedule the interview at the earliest opportunity. Accordingly, the Applicants request the Examiner to refrain from acting on this Preliminary Amendment until the interview can be conducted.

Respectfully submitted,



Daniel J. Stanger
Registration No. 32,846
Attorney for Applicants

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 Diagonal Road, Suite 370
Alexandria, Virginia 22314
(703) 684-1120
Date: May 10, 2006